e) implanting a dopant impurity of arsenic at a dose of approximately 5×10^{15} atoms/cm^2 at an implanting energy of approximately 180 keV into said upper level polysilicon layer being approximately 1000Å thick, thereby conductively doping said layer of upper level polysilicon;

wherein a major portion of implanted conductive impurities reside at the interface between said Upper level polysilicon and said silicided surface, thereby forming resistive contacts between said silicide surfaced lower level conductively doped polysilicon and said conductively doped upper level polysilicon.

8. A process as recited in claim **7**, wherein said conductively doped lower and upper polysilicon are n-type conductivity.

9. A process as recited in claim **7**, wherein said conductively doped lower and upper polysilicon are p-type conductivity.

10. A process as recited in claim **7**, wherein said semiconductor device is a memory semiconductor device.

11. A process as recited in claim **10**, wherein said memory semiconductor device is an SRAM.

12. A process as recited in claim **7**, wherein said metal is selected from the group consisting of titanium, cobalt, platinum, tungsten, molybdenum, palladium and tantalum.

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